CLAIMS

1. A packet switch, comprising:

N input buffer sections, provided corresponding to N input lines, for storing a packet input through the corresponding input lines;

α scheduler sections for determining one of M output lines as a destination of the packet stored in each of said N input buffer sections by a scheduling process independently performed by each scheduler section; and

a switch section for outputting the packet output from each of said N input buffer sections to the destination output line determined by said scheduler section,

wherein said N input buffer sections cyclically use results of scheduling processes by said α scheduler sections.

2. The packet switch according to claim 1, wherein:

said scheduling process is performed by said scheduler section corresponding to a scheduling request notification transmitted from said N input buffer sections; and

each of said N input buffer sections distributes the scheduling request notifications among said scheduler sections as a destination.

3. The packet switch according to claim 2, wherein said input buffer sections have M queues storing packets to be transmitted to the M output lines, and said scheduler sections, which are destinations of the scheduling request notifications, cyclically correspond to the M numbers of each queue.

4. The packet switch according to claim 2, wherein said input buffer sections have said scheduler sections, which are destinations of the scheduling request notifications, cyclically correspond to the each input lines.

5. The packet switch according to claim 2, wherein said input buffer sections have said scheduler sections, which are

destinations of the scheduling request notifications, cyclically correspond to each of a unit time.

6. The packet switch according to claim 2, wherein said input buffer sections check a number of unassigned scheduling request notifications for each of said α scheduler sections, and transmit a next scheduling request notification to the scheduler section having smaller number of scheduling request notifications.

7. The packet switch according to claim 2, wherein said input buffer sections manage a number of scheduling request notifications transmitted to each of said α scheduler sections, and delay an operation of transmitting the scheduling request notification to the scheduler section whose number of the scheduling request notifications has reached a predetermined value until the number becomes smaller than the predetermined value.

8. The packet switch according to claim 1, wherein when a time required by said scheduler section to perform the scheduling process is L times as long as a shortest transmission interval of the packet, the number α of scheduler sections is set to a value equal to or larger than the multiple L.

9. The packet switch according to claim 8, wherein:

L-α is set to a value equal to or larger than 1; and

said N input buffer sections cyclically use results of all scheduling processes of said α scheduler sections.

10. The packet switch according to claim 8, wherein:

L-α is set to a value equal to or larger than 1; and

L-α scheduler sections are used as a redundant system, and said scheduler sections in the redundant system replace when a scheduler section which is not included in the sections in the redundant system becomes faulty.

11. The packet switch according to claim 1, wherein said number α of said scheduler sections and the time of the scheduling

process are set variable depending on the number N of the input lines and the number M of the output lines.

12. The packet switch according to claim 1, wherein said scheduler section performs the scheduling process including an unused line, and performs a re-reading process among the actually used input and output lines and the unused lines, thereby obtaining a plurality of scheduling process results by performing one scheduling process.